Amended Claims under Article 19(1)

1. (Amended) A wide band modulation PLL comprising:

a PLL portion including a voltage control oscillator, a divider for dividing an output signal of the voltage control oscillator, a phase comparator connected to a post stage of the divider, and a loop filter for averaging an output of the phase comparator;

a first modulation input portion for inputting a first modulation signal to the voltage control oscillator to modulate based on an inputted modulation data; and

a second modulation input portion for inputting a second modulation signal to a position of the PLL portion different from the voltage control oscillator based on the modulation data;

wherein the voltage control oscillator includes a first control terminal inputted with the first modulation signal and a second control terminal inputted with a signal based on the second modulation signal;

wherein the first modulation input portion and the second modulation input portion are respectively inputted with a first calibration data and a second calibration data in controlling a modulation degree; and

wherein the modulation degree of the first modulation input portion is controlled by comparing signals based on

outputs from the voltage control oscillator when the first calibration data and the second calibration data are inputted.

2. (Amended) The wide band modulation PLL according to Claim 1;

wherein the first calibration data is a sine wave signal outside of a PLL band and the second calibration data is a sine wave signal in the PLL band.

3. (Amended) The wide band modulation PLL according to claim 1 or claim 2;

wherein maximum frequency deviations of the first calibration data and the second calibration data are equal to each other.

4. (Amended) The wide band modulation PLL according to Claim 3;

wherein the modulation degree of the first modulation input portion is controlled based on a difference between the maximum frequency deviations of the signals based on outputs of the voltage control oscillator when the first calibration data is inputted and when the second calibration data is inputted.

5. (Amended) The wide band modulation PLL according to any

one of Claims 1 through 4;

wherein the second modulation portion includes dividing ratio generating means for controlling a dividing ratio of the divider based on a carrier frequency data and the modulation data.

6. (Amended) The wide band modulation PLL according to any one of Claims 1 through 4;

wherein the second modulation portion includes a direct digital synthesizer for generating a modulation signal based on a carrier frequency data and the modulation data to output to the phase comparator.

7. (Amended) The wide band modulation PLL according to Claim 6;

wherein the divider includes a plurality of dividers having fixed dividing ratios which are consecutively connected.

8. (Amended) A wireless terminal apparatus comprising the wide band modulation PLL according to any one of Claims 1 through 7.

9. (Amended) A modulation degree control system of a wide band modulation PLL comprising:

the wide band modulation PLL according to any one of Claims 1 through 7;

a demodulator for demodulating an output of the voltage control oscillator of the wide band modulation PLL; and

modulation degree controlling means for outputting a modulation degree control signal to the first modulation input portion of the wide band modulation PLL by controlling a modulation degree based on an output of the demodulator.

10. (Amended) A polar modulation system comprising:

the wide band modulation PLL according to any one of Claims 1 through 7;

an envelope signal generating portion for generating an envelope signal based on an inputted amplitude modulation data; and

a polar demodulator for generating a transmitting output signal based on an output of the voltage control oscillator of the wide band modulation PLL and an output signal of the envelope signal generating portion.

11. (Amended) A modulation degree control system of a polar modulation system comprising:

the polar modulation system according to Claim 10;

a demodulator for demodulating an output of the voltage control oscillator of the wide band modulation PLL; and

modulation degree controlling means for outputting a modulation degree control signal to the first modulation input portion of the wide band modulation PLL by controlling a modulation degree based on an output of the demodulator.

12. (Amended) A method of adjusting a modulation degree of a wide band PLL which is a method of controlling a modulation degree of a wide band modulation PLL comprising a PLL portion including a voltage control oscillator, a divider for dividing an output signal of the voltage control oscillator, a phase comparator connected to a post stage of the divider, and a loop filter for averaging an output of the phase comparator, said method comprising:

a step of inputting a first calibration data to a first control terminal of the voltage control oscillator;

a step of inputting a second calibration data to a position of the PLL portion different from the voltage control oscillator;

a step of demodulating an output of the voltage control oscillator when the first calibration data is inputted;

a step of demodulating the output of the voltage control oscillator when the second calibration data is inputted; and

a step of controlling a modulation degree of a modulation signal inputted to the first control terminal of the voltage control oscillator based on the demodulated signal.

13. (Amended) A method of controlling a modulation degree of a wide band modulation PLL which is a method of controlling a modulation degree of a polar modulation system comprising a wide band modulation PLL including a voltage control oscillator, a divider for dividing an output signal of the voltage control oscillator, a phase comparator connected to a post stage of the divider, and a loop filter for averaging an output of the phase comparator, said method comprising:

a step of inputting a first modulation signal based on a first calibration data to a first control terminal of the voltage control oscillator;

a step of inputting a second modulation signal based on a second calibration data to a position of the PLL portion different from the voltage control oscillator;

a step of synthesizing an output signal of the voltage control oscillator of the PLL portion based on an amplitude modulation data at a polar modulator;

a step of demodulating an output of the polar modulator when the first calibration data is inputted;

a step of demodulating the output of the polar modulator when the second calibration data is inputted; and

a step of controlling a modulation degree of a modulation signal inputted to the first control terminal of the voltage control oscillator based on the demodulated signal.

14. (Deleted)